SpartanMC

Timer Pulse Accumulator Module (timer-pulseacc)

Table of Contents

List of Figures

List of Tables

Timer Pulse Accumulator Module (timer-pulseacc)

The timer pulse accumulator module counts impulses from an external input. The module supports two operation modes: Either it counts impulses on an input called PIN or it counts impulses on RTI input until the next impulse on PIN.

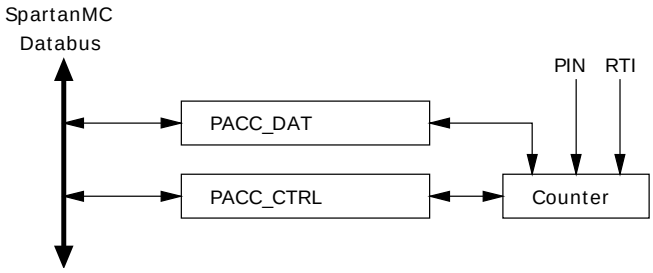

Figure 1: Timer Pulse Accumulator block diagram

In the first operation mode the module counts continously all impulses from the input PIN. In the second mode the counter stops if an impulse on RTI occurs. If the counter has stopped (due to an RTI impulse) a read access to the counter register will clear the counter value. Whereas a read access to the control register always clears the counter value in both operation modes.

Note: The timer pulse accumulator can be used as stand alone peripheral or in connection with an basic timer module (used as impulse source).

1. Module Parameters

Table 1: Timer Pulse Accumulator module parameters

Parameter	Default Value	Descripton
BASE_ADR		Start address of the memory mapped peripheral registers. The value is taken as offset to the start address of the peripheral memory space. **This parameter is set by jConfig automatically.**

2. Peripheral Registers

2.1. Timer Pulse Accumulator Register Description

The timer pulse accumulator peripheral provides two 18 bit registers which are mapped to the SpartanMC address space e.g. 0x1A000 + BASE_ADR + Offset.

Table 2: Timer Pulse Accumulator Registers

Offset	Name	Access	Description
0	PACC_CTRL	read/ write	Specify the operation mode. (An access on this register clears the counter value)
1	PACC_DAT	read	Counter value register.

2.2. PACC_CTRL Register

Table 3: PACC_CTRL register layout

Bit	Name	Access	Default	Description
0	PACC_EN	read/ write	0	If set to one the pulse accumulator logic is enabled.
1	PACC_MODE	read/ write	0	Operation mode: 0 = Count all impulses (raising edges) on input PIN. 1 = Count all impulses (raising edges) on imput RTI until an input on PIN occurs.
2-17	x	read	0	Not used.

Table 3: PACC_CTRL register layout

2.3. PACC_DAT Register

Table 4: PACC Counter register layout

Bit	Name	Access	Default	Description
0-17	Counter	read/ write	x	18 bit counter value.

2.4. PACC C-Header for Register Description

```
#ifndef __COUNTER_H
#define __COUNTER_H

#ifdef __cplusplus
extern "C" {
#endif

#define COUNTER_EN      (1 << 0)
#define COUNTER_MODE   (1 << 1)

#define COUNTER_INPMODE   (COUNTER_MODE * 0)
#define COUNTER_RTIMODE   (COUNTER_MODE * 1)

typedef struct pacc {
   volatile unsigned int control;   // (r/w) reset conter
   volatile unsigned int counter;   // (r)
} counter_regs_t;

#ifdef __cplusplus
}
#endif

#endif
```